

100V N-Channel SGT MOSFET

General Description

• Trench Power SGT technology

- Very low on-resistance R_{DS(ON)}
- Low Gate Charge
- Excellent Gate Charge x R_{DS(ON)} Product

Applications

• High Frequency Switching and Synchronous Rectification

Product Summary

 $\begin{array}{lll} V_{DS} & 100V \\ I_{D} \mbox{ (at V_{GS} = 10V)} & 100A \\ R_{DS(ON)} \mbox{ (at V_{GS} = 10V)} & < 4.8 m\Omega \\ \end{array}$

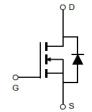
 $R_{DS(ON)}$ (at V_{GS} =4.5V) < 6m Ω

100% UIS Tested 100% DVDS Tested









Part Number	r Package Type Form		Marking	
TSP048N10AT	TO-220	Tube	TSP048N10AT	
TSG048N10AT	DFN5×6	Tape & Reel	TSG048N10AT	

Absolute Maximum Ratings (T_A =25°C unless otherwise noted)

Parameter		Symbol	Maximum	Units	
Drain-Source Voltage		V _{DS}	100	V	
Gate-Source Voltage		V_{GS}	±20	V	
Continuous Drain Current B	T _C =25°C		100	•	
Continuous Drain Current B	T _C =100°C	I _D	71	Α	
Pulsed Drain Current A		I _{DM}	400	Α	
Avalanche Current A		I _{AS}	30	Α	
Single Pulse Avalanche Energy L =0.3mH A		E _{AS}	135	mJ	
Power Dissipation C	T _C =25°C	D	166.5	W	
Power Dissipation ^C	T _C =100°C	P _D	83.4	W	
Junction and Storage Temperature Range		T _J , T _{STG}	-55 to 175	°C	

Thermal Characteristics

Parameter		Symbol Maximum		Units	
Maximum Junction-to-Case Steady-State		$R_{\Theta JC}$	0.9	°C/W	
Maximum Junction-to-Ambient	Steady-State	$R_{\Theta JA}$	50	-C/VV	



LIGCUIC	cal Characteristics(T _J =25ºC ur				\/-!		
Symbol	Parameter	Conditions		Value			Units
				Min	Тур	Max	
STATIC P	ARAMETERS	T				1	
BV _{DSS}	Drain-Source Breakdown Voltage	$I_D = 250 \mu A, V_{GS} = 0 V$		100			V
	Zava Cata Valtaga Drain Current	T _J =25°C				1	μA
I _{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 100V, V_{GS} = 0V$ $T_{J} = 125^{\circ}C$			100		
I _{GSS}	Gate-Body Leakage Current	$V_{DS} = 0V, V_{GS} = \pm 20V$	•			±100	nA
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_{D} = 250 \mu A$		1.1	1.5	2.5	V
Б	Otatia Dunia Ocuma On Besistana	V _{GS} =10V, I _D =30A			4.2	4.8	mΩ
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V _{GS} =4.5V, I _D =30A			5	6	mΩ
g _{FS}	Forward Transconductance	V _{DS} =5V, I _D =20A			54		S
V_{SD}	Diode Forward Voltage	I _S =30A, V _{GS} =0V				1	V
Is	Maximum Body-Diode Continuous Curre	ent ^B				100	Α
DYNAMIC	PARAMETERS						
C _{iss}	Input Capacitance				4070.8		
C _{oss}	Output Capacitance	V _{GS} =0V, V _{DS} =50V, f =1MH _Z			471		pF
C _{rss}	Reverse Transfer Capacitance				10.8		
R_g	Gate Resistance	f=1MH _Z			1.7		Ω
SWITCHIN	NG PARAMETERS						
Q _g (10V)	Total Gate Charge				69.1		
Q _g (4.5V)	Gate Source Charge				35.2		nC
Q_{gs}	Gate Source Charge				21.3		
Q_{gd}	Gate Drain Charge				4.92		
Q _{oss}	Output Charge	V _{GS} =0V,V _{DS} =50V			77.85		
$t_{D(on)}$	Turn-On Delay Time				39.4		
t _r	Turn-On Rise Time	$V_{GS} = 10V, V_{DS} = 50V, I_{D} = 20A,$ $R_{G} = 1.8\Omega$			8.4		ns
$t_{\text{D(off)}}$	Turn-Off Delay Time				79.5		
t _f	Turn-Off Fall Time				12.8		
t _{rr}	Body Diode Reverse Recovery Time	1 -20A di/dt -100A/:			61.6		ns
Q _{rr}	Body Diode Reverse Recovery Charge	- I _F =20A, di/dt =100A/μs			146		nC

- A. Single pulse width limited by maximum junction temperature.
- B. The maximum current rating is package limited.
- C. The power dissipation P_D is based on $T_{J(MAX)}$ =175°C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.

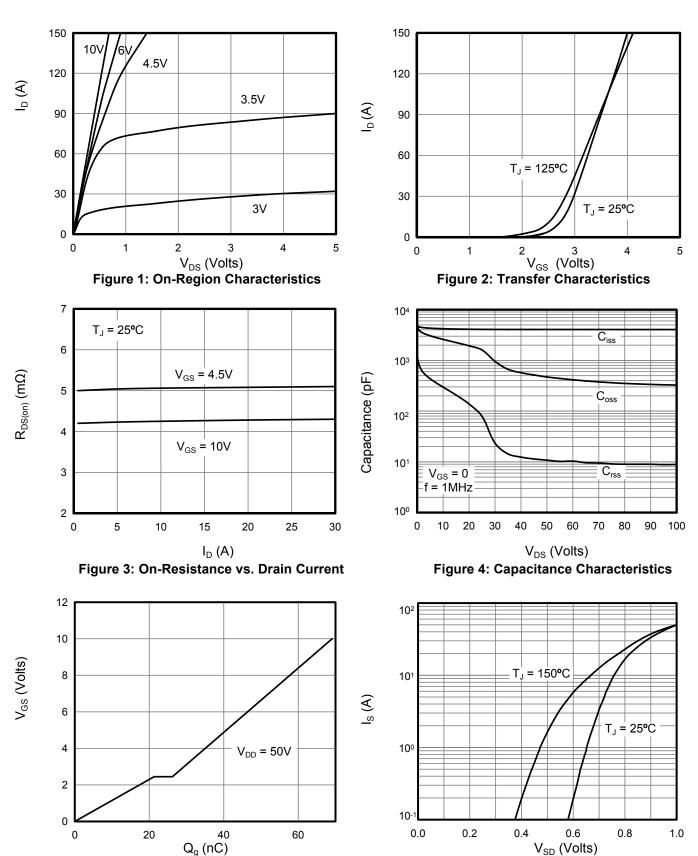
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Figure 6: Body Diode Forward Voltage



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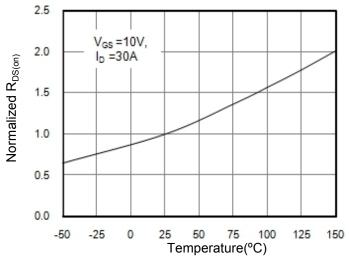
Figure 5: Gate Charge Characteristics



 $Z_{\,\theta\, JC}$ Normalized Transient Thermal Resistance

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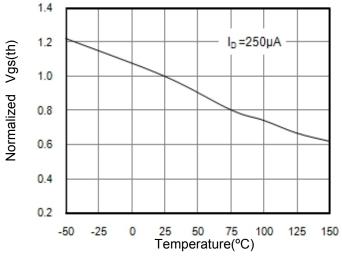
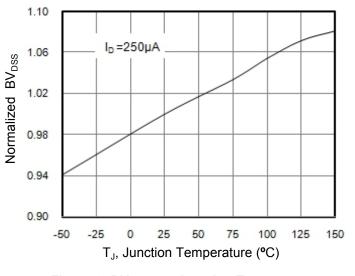


Figure 7: On-Resistance vs. Junction Temperature

Figure 8: Vgs(th) vs. Junction Temperature



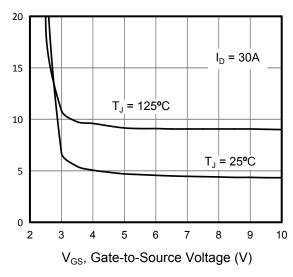
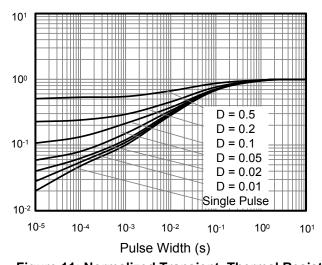


Figure 9: BV_{DSS} vs. Junction Temperature

Figure 10: On-Resistance vs. Gate-Source Voltage



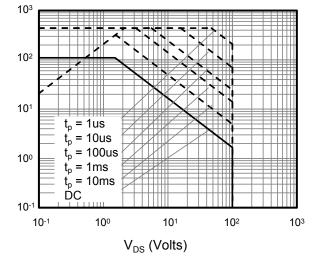


Figure 11: Normalized Transient Thermal Resistance

Figure 12: Safe Operating Area

 $R_{DS(on)}$ (m Ω)

l_D (Amps)



Figure A: Gate Charge Test Circuit and Waveforms

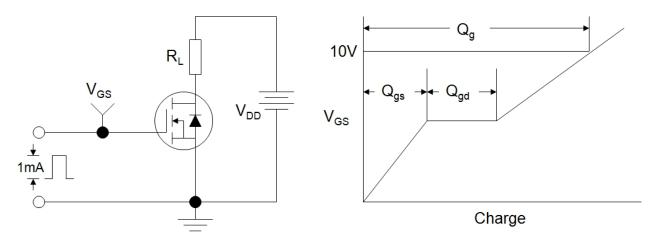


Figure B: Resistive Switching Test Circuit and Waveforms

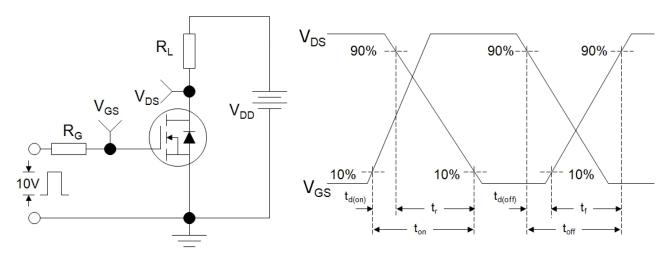
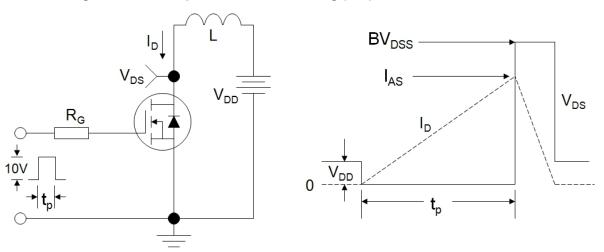


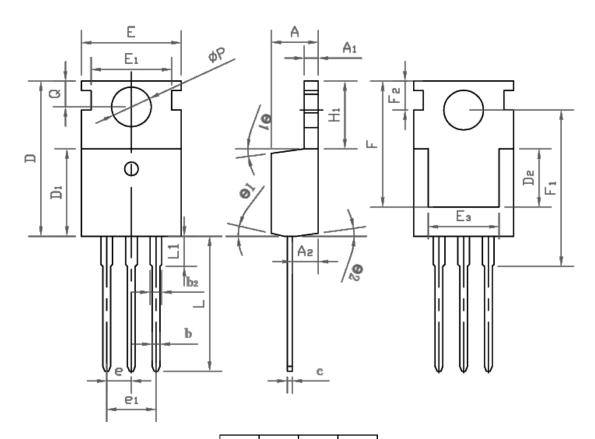
Figure C: Unclamped Inductive Switching (UIS) Test Circuit and Waveforms



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TO-220 (封装厂E)

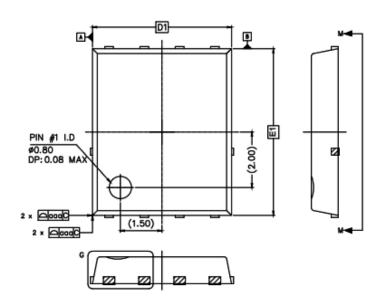


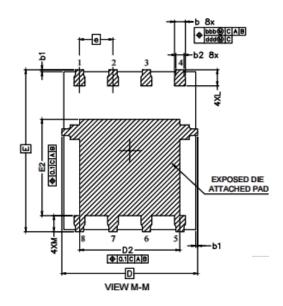
SYMBOL	MIN NOM		MAX	
Α	4.27	4.57	4.87	
Aı	1.15	1.30	1.45	
A₂	2.10	2.40	2.70	
b	0.70	0.80	1.00	
b₂	1.17	1.27	1.50	
С	0.40	0.50	0.65	
D	15.10	15.60	16.10	
D1	8.80	9.10	9.40	
D ₂	5.70	6.70	7.00	
E	9.70	10.00	10.30	
Εı	ı	8.70	1	
E ₂	9.63	10.00	10.35	
Ез	7.00	8.00	8.40	
е	2.54 BSC			
e_1	5.	08 BS	С	
H1	6.00	6.50	6.85	
L	12.75	13.50	13.90	
L1	-	3.10	3.40	
ØΡ	3.45	3.60	3.75	
Q	2.60	2.80	3.00	
O 1	4*	7*	10°	
Θ_2	0*	3*	6*	
F	13.30	13.50	13.70	
F1	15.50	15.90	16.30	
F ₂	2.80	3.00	3.20	

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DFN5x6(封装厂A)





SYMBOL	MIN	MAX	SYMBOL	MIN	MAX
A	0.95	1.05	aaa	0.10	
A1	0.00	0.05	ЬЬЬ	0.10	
A3	0.25 REF		ccc	0.10	
ь	0.31	0.51	ddd	0.05	
ы	0.03	0.13	cee	0.08	
b2	0.21	0.41			
D	5.15 BSC				
D1	5.00 BSC				
D2	3.70	3.90			
E	6.15 BSC				
E1	6.00 BSC				
E2	3.56	3.76			
e	1.27 BSC				
L	0.51	0.71			
М	0.51	0.71			
P	10°	12°			

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